REMARKS

Claims 2, 4, 10, 12, 14, and 20 have been amended. No new matter has been added. Claims 1-20 and 47 are pending in the present application. In the Office Action, claims 1, 7, 11, 17, and 47 were rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Yu (U.S. Patent No. 6,255,175). The Examiner's rejections are respectfully traversed.

With respect to independent claims 1, 11, and 47, Applicants describe and claim, among other things, forming a gate dielectric above a surface of the substrate and forming a doped-poly gate structure above the gate dielectric, the doped-poly gate structure having an edge region. Applicants also describe and claim forming a first dopant-depleted region in the edge region of the doped-poly gate structure adjacent the gate dielectric and a second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure. In one embodiment, set forth in dependent claims 7 and 17, forming the first and second dopant-depleted regions includes depleting the edge region of the doped-poly gate structure adjacent the gate dielectric by forming depleting dielectric spacers adjacent the doped-poly gate structure and depleting the substrate under the edge region of the doped-poly gate structure by forming the depleting dielectric spacers. By forming the second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure, parasitic Miller capacitance may be reduced.

Yu describes forming a MOSFET 200 including a gate structure 206 formed above a substrate 102. Source and drain extensions 212, 214 are formed in the substrate such that a portion of the source and drain extensions 212, 214 extend beneath the gate structure 206. To minimize a parasitic Miller capacitance between the gate structure 206 and the source and drain extensions 212, 214, Yu describes forming first and second depletion regions 232, 234 by counter-doping sidewalls of the gate structure 206. However, Yu does not describe or suggest

forming a second dopant-depleted region in the substrate under the edge region of the doped-poly gate structure.

In the FINAL Office Action, the Examiner alleges that the source and drain extensions 212, 214 extending beneath the gate structure 206 are second dopant-depleted regions formed in the substrate 102 under the edge region of the doped-poly gate structure 206. Applicants respectfully disagree and note that Yu states that the source and drain extensions 212, 214 are doped regions having source and drain overlaps 222, 224 that result in parasitic Miller capacitance. See Yu, col. 4, ll. 1-32 and Figure 3. Moreover, Yu is completely silent with regard to depleting the substrate under the edge region of the doped-poly gate structure by forming depleting dielectric spacers. Thus, Applicants respectfully submit that claims 1, 7, 11, 17, and 47 are not anticipated by Yu and request that the Examiner's rejections of these claims under 35 U.S.C. § 102(e) be withdrawn.

In the Office Action, the Examiner stated that claims 2-6, 8-10, 12-16, and 18-20 would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Pursuant to the aforementioned amendments, Applicants respectfully submit that claims 2-6, 8-10, 12-16, and 18-20 are in condition for allowance.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

Date: 12/10/03

Mark W. Sincell, Reg. No. 52,226
Williams Morgan & Amerson, P.C.
10333 Richmond Avenue, Suite 1100
Houston, TX 77042
(713) 934-7000
(713) 934-7011 (Fax)

AGENT FOR APPLICANTS